ATOMIC IP CORE

ARINC 818 IP Core and Evaluation Packages

The A818 Atomic IP Core is a powerful and flexible intellectual property (IP) core that enables you to quickly and easily implement ARINC 818-3 connections into your hardware. With support for ARINC 818 link rates up to 10.0 Gbps, this IP core is compatible with most Xilinx and Intel (Altera) FPGAs, as well as the MicroSemi PolarFire FPGA.

This Core is delivered with a reference design project and a development board for your desired FPGA, giving you a working ARINC 818 platform to begin adapting to your unique requirements.

The IP Core is designed to meet the highest safety standards and is offered in an Airborne package that includes source code, testing artifacts, and other documentation needed to support your DO-254 certification effort.

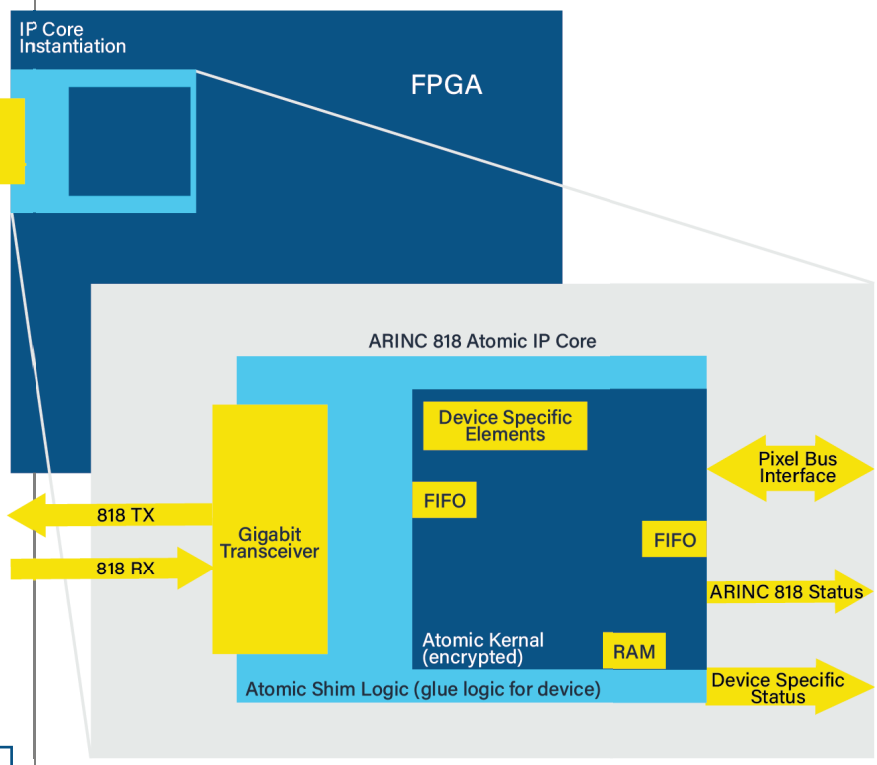
APPLICATIONS:

- Single or Multiple Channel FPGAs
- Channel Bonded Links
- ARINC 818 Switches
- Video Concentrators

INCLUDED:

- ARINC 818 Atomic Kernel - Encrypted VHDL
- Reference Design and additional FPGA "Shim" logic - Unencrypted VHDL
- Development Board for specified FPGA
  - Altera, Xilinx, or Microsemi hardware pre-configured for ARINC 818
  - 850nm FO SFP provided
  - Working Reference Design for Vivado, Quartus, or Leonardo
  - Reference design pre-loaded into delivered development board
  - Transmits test pattern on ARINC 818
  - Receives and re-transmits ARINC 818
- User Manual
- IP Integration Guidelines
- 20 Hours of Technical Support
- R&D License using SignOnce agreement

Production Licenses Sold Separately



FEATURES: The ARINC 818 Atomic IP Core is compile-time configurable to match the specific requirements of your ARINC 818 video format. Features and supported formats include:

Video Resolution and Frame Rates	Configurable for almost any video resolution and frame rate
ARINC 818 Link Speeds	1X, 2X, 3X, 4X, 5.0 Gbps, 6X, 8X, and 10.0 Gbps
Pixel Packing/Unpacking Types	RGB 8:8:8, ARGB 8:8:8:8, RGB 5:6:5, Mono 8-bit, "No Pack" for any pre-packaged pixel type
Video Types	Compatible with progressive and interlaced video
Pixel Interface	Provides simple 32-bit pixel bus transmit and receive ports with independent pixel clocks
Latency	Less than one video line time on receive and transmit
Line Synchronization/Segmentation	Line-synchronous or non-line synchronous transmission; Configurable for desired pixels per line
Object 0 Ancillary Data	Supports real-time update of transmitter's Obj 0 data; Setting default Obj 0 transmit data at compile-time; Complete Obj 0 data recovery by receiver
Receiver Error and Status	Provides receiver status and error detection indicators
Instantiation Options	Transmitter only, receiver only, or full-duplex transceiver

greatrivertech.com 4910 Alameda Blvd NE, Albuquerque NM, 87113 RevG 08032023

Phone 505.881.6262 ■ Toll Free 866.478.4491 info@greatrivertech.com

FPGA SUPPORT:

The ARINC 818 Atomic IP Core can be purchased for the FPGAs below. If you do not see your FPGA listed, please contact Great River.

FPGA	Included Development Board	Availability
Altera Arria V	Intel DK-START-5AGXB3N	Upon Demand
Altera Arria X	Intel DK-DEV-10AX115S-A	Immediately
Altera Stratix V	Intel DK-DEV-5SGXEA7N	Upon Demand
Altera Cyclone V	Intel DK-DEV-5CGTD9N	Upon Demand
Altera Cyclone V	T45TerasicP0150	Immediately
Altera Cyclone X	Intel DK-DEV-10CX220A	Immediately
Xilinx Spartan-6	Xilinx DK-S6-EMBD-G	Upon Demand
Xilinx Artix-7	Xilinx EK-A7-AC701-G	Immediately
Xilinx Kintex-7	Xilinx EK-K7-KC705-G	Immediately
Xilinx Kintex-Ultrascale	Xilinx EK-U1-KCU105-G	Immediately
Xilinx Kintex-Ultrascale Plus	Xilinx EK-U1-KCU116-G	Immediately
Xilinx Virtex-6	Xilinx EK-V6-ML605-G	Upon Demand
Xilinx Zynq	Xilinx EK-Z7-ZC706-G	Immediately
Xilinx Zynq-Ultrascale Plus	Xilinx EK-U1-ZCU106-G	Immediately
Xilinx Virtex Ultrascale	Xilinx EK-U1-VCU108-G	Immediately
Xilinx Virtex Ultrascale Plus	Xilinx EK-U1-VCU118-G	Upon Demand
Xilinx Virtex 7	Xilinx EK-V7-VC707-G	Upon Demand
Microsemi PolarFire	Microsemi MPF300-EVAL-KI	Upon Demand

AVAILABLE PACKAGES:

Package	Description
Encrypted IP Core	Ideal for Engineering Teams developing an ARINC 818 FPGA and equipment. *Includes: Altera, Xilinx, or Microsemi Development Board with Reference Design*
Transmitter Development	Ideal for Engineering Teams developing an ARINC 818 transmitter. *Includes: encrypted IP Core, Development board, and the Video Protocol Analyzer (VPA)*
Receiver Development	Ideal for Engineering Teams developing an ARINC 818 receiver. *Includes: encrypted IP Core, Development board, and the XF Tuner*
Total Development	Ideal for Engineering Teams developing both an ARINC 818 transmitter and receiver. *Includes: encrypted IP Core, Development board, the Video Protocol Analyzer (VPA), and the XF Tuner*
Airborne Package *For those having already purchased an initial IP Core product ONLY*	Designed to support customers in obtaining DO-254 safety certification for their FPGAs and hardware. Includes VHDL source code, additional documentation, and additional testing artifacts. Provides a reliable path to DO-254 certification.